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APPLICATION NUMBER: *60/372,172*
FILING DATE: *April 12, 2002*

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EL915426721US

JC654 U.S. PTO
04/12/02

JC879 U.S. PTO
60/372172
04/12/02

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Ionel D.	Jitaru	Tucson. Arizona

☐ Additional inventors are being named on the _______ separately numbered sheets attached hereto

TITLE OF THE INVENTION (500 characters max)

SOFT SWITCHING CONVERTER USING CURRENT SHAPING

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

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ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification *Number of Pages* 7 ☐ CD(s), Number

☒ Drawing(s) *Number of Sheets* 4 ☒ Other (specify) Postcard

☐ Application Data Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☐ Applicant claims small entity status. See 37 CFR 1.27.

☒ A check or money order is enclosed to cover the filing fees

☐ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number:

☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE AMOUNT ($) $160.00

The Invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☐ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: ____________

Respectfully submitted,

SIGNATURE [signature]

Date 4/12/02

TYPED or PRINTED NAME Thomas D. MacBlain

REGISTRATION NO. *(if appropriate)* 24,583

TELEPHONE 602-530-8088

Docket Number: 14609-0003

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

Docket No. 14609-0003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ionel Jitaru, et al.

Serial No.:

Filed: Herewith

For Provisional Patent Application Entitled: SOFT SWITCHING CONVERTER USING CURRENT SHAPING

CERTIFICATE OF MAILING BY EXPRESS MAIL

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Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

Dear Commissioner:

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Washington, D.C. 20231

on

4/12/02
Date

Suzanne Shields
Suzanne Shields

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04/12/02 JC654 U.S. PTO

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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 160

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Jitaru
Examiner Name	
Group Art Unit	
Attorney Docket No.	14609-0003

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account:

Deposit Account Number: 07-0135

Deposit Account Name:

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☐ Charge fee(s) indicated below ☐ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	160

SUBTOTAL (1) ($) 160

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X		=	
Independent Claims		-3** =		X		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) ______

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($)

SUBMITTED BY

				Complete *(if applicable)*	
Name *(Print/Type)*	Thomas D. MacBlain	Registration No. (Attorney/Agent)	24,583	Telephone	602-530-8088
Signature	[signature]			Date	4/12/02

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Soft Switching Converter Using Current Shaping

Background of Invention

1. *Field of the Invention*

This invention relates to DC-to-DC converters, DC-to-AC inverters and AC-to-DC converters. The major characteristic of this power conversion technique is that primary switching elements switches at zero voltage and the secondary rectifiers means have negligible reverse recovery losses.

2. *Description of the Prior Art*

There is a continuing industry demand for increasing power density, which means more power transferred in a given volume. A method for increasing the power transfer through the converter is to increase the switching frequency in order to minimize the size of the transformer and the capacitors. Using prior art topologies such as forward or flyback, which employ "hard" switching techniques, makes high frequency operation less efficient. The switching losses associated with switching elements, which turn on when there is a voltage across them, are proportional with the switching frequency. An increase in switching frequency leads to an increase in switching losses and an increase in level of electromagnetic interference (EMI).

In order to overcome limitations in switching speeds, the prior art has devised a new family of soft transition. The U.S. patent Nos. 5,132,889, 5,126,931, 5,231,563, 5,434,768 present several methods of accomplishing zero voltage switching across the primary switches.

Another power loss mechanism is due to the reverse recovery in the output rectifiers. During switching when a negative polarity voltage is applied to a rectifier that is in conduction, the current through the rectifier will continue to conduct until all the carriers in the rectifier's junctions are depleted. During this period of time the current polarity will reverse the current flowing from the cathode to the anode, while the voltage across the diode is still positive from the anode to the cathode. The current flowing in reverse through the diode will reach a peak value referred in literature as Irrm. Further on,

while the rectifiers' junction is depleting the carriers, the rectifier becomes a high impedance device. The current through the rectifier will decrease rapidly from Irrm level to zero. During the same time the negative voltage across the rectifier will build up to high levels.

During the period of time when there is a negative voltage across the diode and negative current is flowing through it, there will be power dissipation in the device. This kind of loss is referred in the literature as reverse recovery losses. The reverse recovery loss is proportional with the reverse recovery current Irrm, the negative voltage across the rectifier and the frequency.

The reverse recovery current Irrm, which is a key component in reverse recovery loss, is a function of the type of device, the temperature and the current slope at turn off. The reverse recovery characteristics are worse for higher voltage rectifiers. As a result the reverse recovery loss becomes a significant loss mechanism for higher output voltage applications. The reverse recovery current Irrm is directly dependent on the current slope at turn off. A soft slope reduces the reverse recovery current and as a consequence reduces the reverse recovery loss. To accomplish a very soft slope current at turn off an inductive element has to be in series with the rectifier. The inductor element will prevent a fast current variation dI/dt. The presence of an inductive element in series with the rectifier will increase the negative voltage across the rectifier at turn off. The reverse voltage across the rectifier can reach very high levels and can exceed the voltage break down of the device, leading to failure.

RC snubbers or complicated lossless snubbers can be added across the rectifier to reduce the reverse recovery loss and the voltage stress on the devices. This leads to complex circuits and this negatively affects the efficiency and the reliability. As a result of these limitations the high voltage converters have to operate at lower frequency in order to reduce the power dissipation associated with reverse recovery.

In Fig. 2A is presented a standard full bridge phase shifted topology. The primary switching elements, M1, M2, M3 and M4 are controlled as depicted in the key waveforms of Fig. 2B. During the time M1 and M4 are conducting there is a positive voltage at the dot in the secondary winding and the

rectifier D1 is conducting. When M4 turns off in the primary winding the current will continue to conduct and its path will be through the parasitic capacitance of M3 and M4, discharging the parasitic capacitance across M3 to zero and as a result creating zero voltage switching conditions. As a result M3 will turn on at zero voltage. Further M1 and M3 will be conducting. During this time the primary winding of the transformer is shorted and the voltage in the secondary winding is zero. Both D1 and D2 will conduct during this time. The current through Lo will be split equally between D1 and D2.

At the moment when M1 turns off, the current will continue to flow in the primary discharging the parasitic capacitance of M2 towards zero. If certain conditions are met, M2 will turn on at zero voltage conditions. In any event, when M3 and M2 conduct the polarity will change in the secondary winding. The change in polarity will force the current flowing through Lo to flow totally through D2 and the rectifier D1 will be reverse biased. Due to the reverse recovery characteristic of D1 the current will flow in reverse through D1 until the carriers in the junction are depleted. After that the rectifier D1 will behave as a high impedance device. As a function of the current slope through D1 at turn off, which determines the reverse recovery characteristics of D1, and as a function of the parasitic inductive elements in series with D1, large voltage spikes will develop across D1 as shown at 10 in Fig. 2B. This phenomenon will lead to reverse recovery losses in D1, when the reverse recovery current and reverse voltage will be present on the rectifier. In addition, these large voltage spikes developed across D1 may lead to voltage stress, which may exceed the rating of the device. For this reason snubbing circuits may have to be employed across D1, which will increase the power dissipation, increase circuit complexity, decrease reliability and decrease power density. The reverse recovery current associated with D1 will also create a "temporary short" across the secondary winding, preventing the resonant transition across M2 from achieving zero voltage switching conditions. The voltage ringing across D1 will also lead to increased EMI.

The losses associated with the reverse recovery of the output rectifiers are proportionate with the frequency. The trend towards miniaturization requires an increase in switching frequency, which will

lead to more reverse recovery losses. In order to accomplish miniaturization, higher efficiency is necessary to minimize heat. In conclusion we need a topology wherein the reverse recovery losses shall be eliminated, in this way allowing an increase in switching frequency without a penalty in efficiency.

Brief Summary of the Invention

This invention presents a circuit technique designed to reduce the negative impact of the reverse recovery in the rectifiers, while allowing zero voltage switching on the primary switching elements. This technique works by forcing the current out of the rectifier before a reverse voltage is applied to it. This method operates by shaping the current through the output rectifiers using an additional AC voltage source superimposed on the main AC voltage induced in the secondary winding by the primary winding. In this implementation the reverse recovery losses in the rectifiers are totally eliminated, though the converter operates in continuous conduction mode. Another major advantage of the proposed circuit is the fact that the current reflected in the primary is shaped to a trapezoidal form with a low dI/dt during the turn on of the primary switchers. This will allow the completion of the resonant transition to zero voltage across the primary switching elements.

The above and further objects and advantages of the invention will be better understood from the following detailed description of at least one preferred embodiment of the invention, taken in consideration with the accompanying drawings.

Brief Description of the Drawings

Figure 1A is a schematic diagram of a converter utilizing the power transfer methodology of the invention;

Figure 1B is a timing diagram of the circuit of Fig. 1A;

Figure 2A is a schematic diagram of a converter wherein a prior art technique is illustrated;

Figure 2B is a timing diagram of the circuit of Fig. 2A;

Figure 3A is a schematic diagram of a specific exemplary embodiment of a converter configured in accordance with this invention;

Figure 3B is a timing diagram of the circuit of Fig. 3A; and

Figure 4 is a schematic diagram of a further specific embodiment of a converter configured in accordance with this invention.

Detailed Description

The present invention addresses the goal of eliminating the reverse recovery losses, while maintaining continuous conduction mode in the output choke. The general concept is described in connection with Fig. 1A. It consists in adding an additional AC voltage source, which will generate a low voltage square waveform signal.

In Fig. 1A is presented a simplified schematic and in Fig. 1B is presented key waveforms for the technology according to this invention. The circuit is based on a typical full bridge phase shifted topology, with an additional low voltage AC source 15 placed in series with a primary winding 16.

In Fig. 1B the conventional control signals for the primary switching elements M1, M2, M3 and M4 are also depicted. The injected AC voltage will alter the voltage in the secondary of the transformer as is depicted by the dotted lines in Fig. 1B, Vsec.

During the time wherein M1 and M4 are conducting the voltage induced in the secondary winding has a positive polarity at the dot and D1 is conducting. When M4 ceases to conduct, the injected voltage 17 of the source 15 produces a voltage 18 in the secondary winding with a low amplitude and negative polarity at the dot. This will force the current out of D1 and into D2. Without the injected voltage 16 the current through Lo would be equally split between D1 and D2.

At the time when M1 will be turned off and M2 will be turned on, the voltage induced in the secondary winding will change polarity, creating a negative voltage at the dot. This will not change the current flow in the secondary, because D2 is already in full conduction. Without the injected voltage at this time both D1 and D2 would be in full conduction and the negative voltage induced in the secondary

winding would be applied to D1 leading to reverse recovery current and as a result reverse recovery losses.

In Fig. 3A is presented the implementation circuit. The additional injected voltage is implemented by using a small additional transformer 20 in series with the primary winding and an additional capacitor 22. In Fig. 3B the key waveforms are also depicted. The additional magnetic element 20, which has the primary winding in series with the primary winding of the transformer and the secondary winding in series with the capacitor 22, accomplishes several tasks. First it creates the AC signal in series with the primary winding which forces the output rectifier out of conduction during the dead time, before the voltage polarity reverses in the secondary preventing the reverse recovery losses. The second effect is the creation of an additional triangular current injected at the connection between M1 and M2, ensuring zero voltage switching conditions even at light load.

Furthermore, in Fig. 4, the diodes D1 and D2 are replaced with synchronous rectifiers. One of the limitations associated with synchronous rectification is the conduction of the body diode, when the synchronous rectifier is turned off before the voltage polarity changes. In this way the current will flow through the body diode when the polarity changes in the secondary. The reverse recovery characteristics of the body diode are worse than ultra fast rectifiers. The advantage of a lower voltage drop on the rectifier means is offset by the additional reverse recovery losses. This problem will get worse in higher voltage applications, larger than 24V, wherein the reverse recovery loss mechanism is the dominant rectification loss. In the present invention wherein the reverse recovery losses are eliminated, it is very beneficial to replace the diodes with synchronous rectifiers.

The foregoing descriptions of at least one preferred embodiment are exemplary and intended to limit the claimed invention. Obvious modifications that do not depart from the spirit and scope of the invention as claimed will be apparent to those skilled in the art.

I claim:

1. A power conversion circuit having a power transformer, four semiconductor switching elements connected as a bridge across an input to the power conversion circuit and connected to a primary winding of the power transformer to reverse current through the primary winding, a split secondary winding on the power transformer, a first unidirectional current conducting device connected from one end of the split secondary winding to an inductor, a second unidirectional current conducting device connected from a second end of the split secondary winding to the inductor, the inductor and a connection to an interconnection between two halves of the split secondary winding being connected to an output of the power conversion circuit, an injection voltage source connected to the primary winding of the power transformer for applying an injection voltage to the primary winding in addition to an input voltage to the primary winding via the semiconductor switching elements connected to a bridge.

2. The power conversion circuit according to claim 1, wherein the injection voltage source is a winding on an injection voltage transformer, said winding being connected in series with said primary winding of the power transformer.

3. The power conversion circuit according to claim 2, wherein the injection voltage transformer has a further winding connected to a capacitor.

4. The power conversion circuit according to claim 1, wherein the unidirectional current conducting devices are semiconductor switching devices.

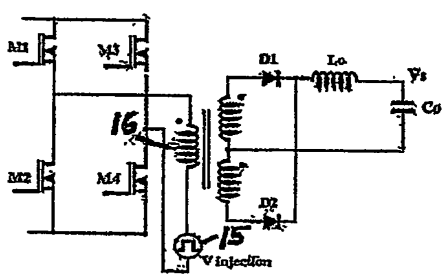

Figure 1A

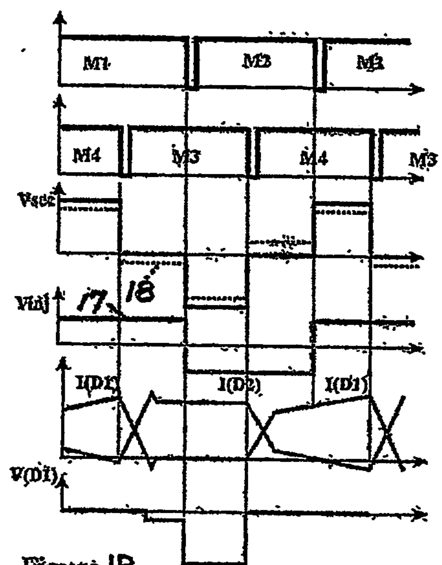

Figure 1B

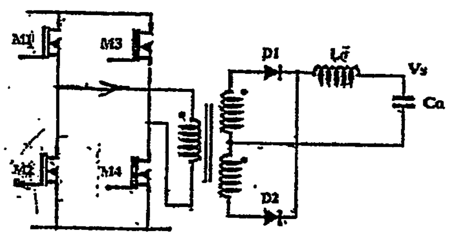

Figure 2A

Prior art

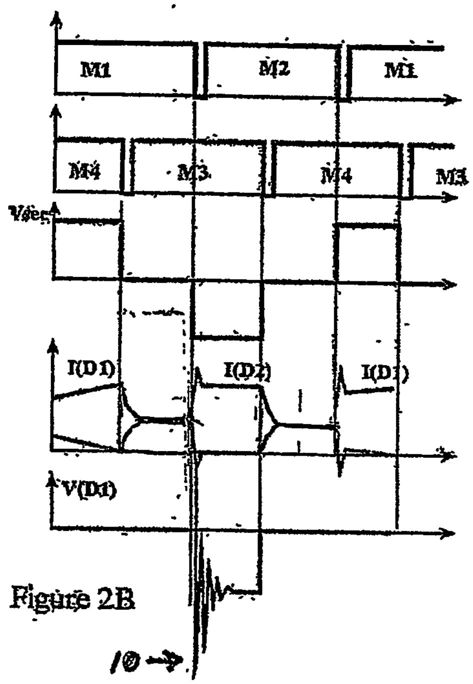

Figure 2B

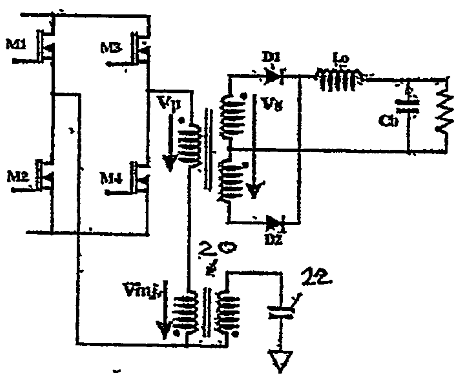

Figure 3A

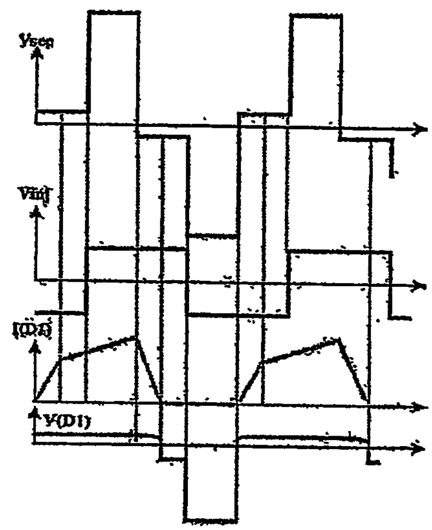

Figure 3B

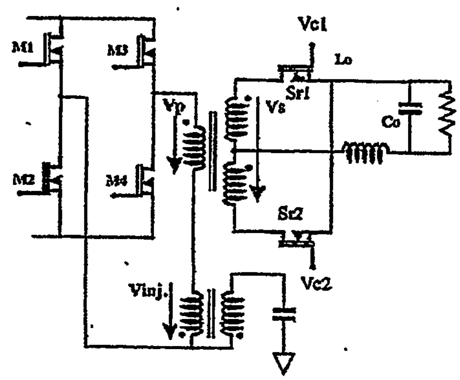

Figure 4